This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A semiconductor package for a micro-machined semiconductor device, comprising:

a) a substrate having a first surface and a second surface, the micro-machined semiconductor device located adjacent the first surface;

b) a plurality of vias, extending through the substrate between the first and second surfaces;

c) an electrical connection located between the vias and the micro-machined semiconductor device for electrically connecting the vias to the semiconductor device;

d) a solder seal, located between the micro-machined semiconductor device and the first surface for hermetically sealing the micro-machined semiconductor device;

e) a plurality of ultrasonically deposited wire bond bumps ~~rigid support~~ located between the micro-machined semiconductor device and the first surface for supporting the micro-machined semiconductor device during assembly and preventing the micro-machined semiconductor device from contacting the first surface, the wire bond bumps formed from either gold or a gold alloy; and

f) a plurality of solder spheres mounted to the second surface and electrically connected to the vias.

2. (original) The semiconductor package according to claim 1, wherein the electrical connection includes:

a) a first pad located on the micro-machined semiconductor device; and

b) a second pad located on the first surface; and

c) a solder joint connected between the first and second pad.

3. (original) The semiconductor package according to claim 1, wherein the substrate is a low temperature co-fired ceramic.

4. (original) The semiconductor package according to claim 1, wherein the seal is a ring of solder located adjacent an outer perimeter of the substrate.

5 - 8. (canceled)

9. (original) The semiconductor package according to claim 3, wherein the substrate has a plurality of layers.

10. (currently amended) The semiconductor package according to claim ~~10~~ 9, wherein a plurality of circuit lines are located on the layers, the circuit lines connected between the vias.

11. (original) The semiconductor package according to claim 1, wherein a ball pad is attached to the second surface, the solder sphere attached to the ball pad.

12. (original) The semiconductor package according to claim 11, wherein the solder sphere is attached to the ball pad by a reflowed solder paste.

13. (currently amended) A semiconductor package for a micro-machined semiconductor device comprising:

a) a low temperature co-fired ceramic substrate having a plurality of layers, the substrate having a top and a bottom surface;

b) a plurality of vias, extending between the layers;

c) a plurality of solder spheres, located on the bottom surface and electrically connected to the vias;

d) a plurality of ~~rigid supports~~ ultrasonically deposited wire bond bumps, attached to the top surface, the wire bond bumps formed from either gold or an alloy of gold;

e) a solder seal ring located between the micro-machined semiconductor device and the top surface, around an outer perimeter of the substrate, the seal ring hermetically sealing the micro-machined semiconductor device;

f) the micro-machined semiconductor device spaced from the top surface by the ~~rigid supports~~ wire bond bumps such that a movable portion of the micro-machined semiconductor device is unconstrained for movement, the ~~rigid supports~~ wire bond bumps preventing the micro-machined semiconductor device from contacting the top surface during assembly; and

g) an electrical connection located between the vias and the micro-machined semiconductor device for electrically connecting the vias to the semiconductor device.

14. (original) The semiconductor package according to claim 13, wherein the electrical connection includes:

a) a first pad located on the micro-machined semiconductor device; and

b) a second pad located on the top surface; and

c) a solder joint connected between the first and second pad.

15 - 18. (canceled)

19. (original) The semiconductor package according to claim 13, wherein a plurality of circuit lines are located on the layers, the circuit lines connected between the vias.

20. (original) The semiconductor package according to claim 13, wherein a ball pad is attached to the bottom surface, the solder sphere attached to the ball pad.

21. (original) The semiconductor package according to claim 13, wherein the solder sphere is attached to the ball pad by a reflowed solder paste.

22. (previously withdrawn)A method of making a semiconductor package comprising the steps of:

a) punching vias in at least two low temperature co-fired ceramic layers;

b) filling the vias with a conductor;

c) screen printing conductor lines on the layers;

d) screen printing a seal ring and a plurality of pads on one of the layers;

e) screen printing a plurality of ball pads on one of the layers;

f) stacking the layers;

g) laminating under pressure the layers into a substrate;

h) firing the substrate in an oven;

i) depositing a rigid support on the substrate;

j) screening a first solder paste onto the seal ring and the pads;

k) placing a micro-machined semiconductor device onto the substrate;

l) reflowing the first solder paste in an oven such that the micro-machined semiconductor device is attached to the substrate;

m) screening a second solder paste onto the ball pads;

n) placing a plurality of solder spheres onto the ball pads; and

o) reflowing the second solder paste in an oven such that the solder spheres are attached to the ball pads.

23. (previously withdrawn) The method according to claim 22, wherein the rigid support is an ultrasonically deposited metal.

24. (previously withdrawn) The method according to claim 22, wherein the metal is chosen from the group consisting of:

a) gold; and

b) an alloy of gold and palladium.